

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Hisaya MORI, et al.

Serial No.:

Group Art Unit:

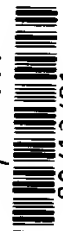
Filed: August 13, 2001

Examiner:

For: APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED  
CIRCUIT

JC997 U.S. PTO

09/927368



08/13/01

**INFORMATION DISCLOSURE STATEMENT**Commissioner for Patents  
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

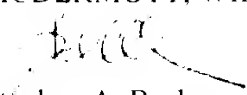
This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The Examiner's attention is directed to co-pending U.S. Patent Application Serial No. 09/904,625, filed July 16, 2001, which is directed to related technical subject matter. The identification of this U.S. Patent Application is not to be construed as a waiver of secrecy as to that application now or upon issuance of the present application as a patent.

The Examiner is respectfully requested to consider the cited application and the art cited therein during examination.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

  
Stephen A. Becker  
Registration No. 26,527

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
(202) 756-8000 SAB:ykg  
**Date: August 13, 2001**  
Facsimile: (202) 756-8087